IN THE CLAIMS

Please cancel Claims 1, 2, 14, and 20 without prejudice or disclaimer.

Claims 1 and 2 (cancelled).

Claim 3 (currently amended): A write driver circuit having a differential signal input, comprising:

a write head;

an H-switch having a first and second transistor with a first node defined therebetween, and a third and fourth transistor with a second node defined therebetween, wherein said first and second nodes are adapted to drive the write head;

a first boosting transistor set coupled to said differential signal input adapted to pull said first node low and said second node high;

a second boosting transistor set coupled to said differential signal input adapted to pull said first node high and said second node low; and

a pre-driver including a fifth transistor coupled between said differential signal input and said H-switch first transistor, and a sixth transistor coupled between said differential signal input and said H-switch third transistor,

~~The write driver circuit specified in Claim 2~~ wherein said fifth and sixth transistors transient currents during switching, wherein said transient currents drive said first and second boosting transistor set.

Claim 4 (currently amended): The write driver circuit specified in Claim ~~1~~ 3 wherein said first boosting transistor set includes at least one PMOS transistor.

Claim 5 (original): The write driver circuit specified in Claim 4 wherein said first boosting transistor set includes a first and second PMOS transistor.

Claim 6 (original): The write driver circuit specified in Claim 5 wherein said second boosting set includes a pair of PMOS transistors.

Claim 7 (currently amended): A write driver circuit having a differential signal input, comprising:

a write head;

an H-switch having a first and second transistor with a first node defined therebetween, and a third and fourth transistor with a second node defined therebetween, wherein said first and second nodes are adapted to drive the write head;

a first boosting transistor set coupled to said differential signal input adapted to pull said first node low and said second node high; and

a second boosting transistor set coupled to said differential signal input adapted to pull said first node high and said second node low,

wherein said first boosting transistor set includes a first and second PMOS transistor; and

~~The write driver circuit specified in Claim 5~~ wherein said first and second PMOS transistors are coupled in parallel.

Claim 8 (original): The write driver circuit specified in Claim 7 wherein said first PMOS transistor is coupled to said second node, and said second PMOS transistor is coupled to the H-switch first transistor.

Claim 9 (original): The write driver circuit specified in Claim 8 wherein the H-switch is disposed between an upper and lower voltage rail, the first transistor has a base, and wherein said second PMOS transistor is adapted to pull said first transistor base toward said upper voltage rail and said first node toward said lower voltage rail.

Claim 10 (original): The write driver circuit specified in Claim 9 wherein said first PMOS transistor is adapted to pull said second node toward said upper voltage rail.

Claim 11 (currently amended): The write driver circuit specified in Claim ~~1~~ 3 further comprising a first resistor coupled between said first node and said second transistor, and a second resistor coupled between said second node and said fourth

transistor, wherein the sum of said first and second resistor resistance is matched to an impedance of the write head.

Claim 12 (original): The write driver circuit specified in Claim 11 wherein said first and second resistors are matched.

Claim 13 (currently amended): The write driver circuit specified in Claim ~~1~~ 3 wherein said first and second boosting transistor sets are adapted to create both a larger voltage swing and a faster slew rate at said first and second node from that produced by the circuit without said first and second boosting transistor sets.

Claim 14 (cancelled).

Claim 15 (currently amended): The method as specified in Claim ~~14~~ 19 wherein the boosting transistors comprise a pair of PMOS transistors.

Claim 16 (original): The method as specified in Claim 15 wherein a first of the boosting transistors is coupled to one half of the H-switch, and a second boosting transistor is coupled to the other half of the H-switch.

Claim 17 (original): The method as specified in Claim 16 wherein the first boosting transistor pulls the second output up while the second boosting transistor drives the respective half of the H-switch harder to responsively pull down the first output.

Claim 18 (currently amended): The method as specified in Claim ~~14~~ 19 further comprising the step of matching the output impedance of the H-switch to an impedance of the write head driven by the first and second output.

Claim 19 (currently amended): A method of increasing a slew rate and voltage swing at a first and second output of an H-switch adapted to drive a write head, comprising the step of:

utilizing a set of boosting transistors coupled to the H-switch to increase a pull-up voltage at the first output while simultaneously increasing a pull-down voltage at the second output; and

~~The method as specified in Claim 14 further comprising the step of~~ using a pre-driver to drive said H-switch, wherein transient currents of said pre-driver drive said boosting transistors.

Claim 20 (cancelled).

Claim 21 (currently amended): A write driver circuit having a differential signal input, comprising:

an H-switch having a first and second transistor with a first node defined therebetween, and a third and fourth transistor with a second node defined therebetween, wherein said first and second nodes are adapted to drive a write head;

a first boosting transistor coupled to said differential input adapted to pull said first node low and said second node high; and

a second boosting transistor coupled to said differential input adapted to pull said first node high and said second node low,

~~The write driver circuit specified in Claim 20~~ wherein the H-switch is disposed between an upper and lower voltage rail, the first transistor has a base, and wherein said second boosting transistor is adapted to pull said first transistor base toward said upper voltage rail and said first node toward said lower voltage rail.

Claim 22 (currently amended): The write driver circuit specified in Claim ~~20~~ 21 wherein said first boosting transistor is adapted to pull said second node toward said upper voltage rail.

Claim 23 (currently amended): A write driver circuit having a differential signal input, comprising:

an H-switch having a first and second transistor with a first node defined therebetween, and a third and fourth transistor with a second node defined therebetween, wherein said first and second nodes are adapted to drive a write head;

a first boosting transistor coupled to said differential input adapted to pull said first node low and said second node high;

a second boosting transistor coupled to said differential input adapted to pull said first node high and said second node low, and

~~The write driver circuit specified in Claim 20 further comprising~~ a pre-driver coupled to said H-switch, wherein said pre-driver has transient currents driving said first and second boosting transistors.

Claim 24 (original): The write driver circuit specified in Claim 23 wherein said first and second boosting transistors comprise PMOS devices.